Amendments to the Claims:

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor integrated circuit comprising:

a clock input terminal for receiving a clock signal and a data input terminal for receiving a data signal;

an internal clock generating circuit for generating an internal clock signal; ~~which is switched at an intermediate timing between the i-th (i: an integer of 1 or larger) switch timing and the (i+1)th switch timing of the clock signal input to said clock input terminal; and~~

a latch circuit for latching the data signal input to said data input terminal synchronously with said internal clock signal; and

means for preventing a timing margin, at a time of latching the data signal synchronously with said internal clock signal, from being decreased in a case where a duty ratio of the clock signal input to the clock input terminal is different than 50%, said means including means for switching the internal clock signal at an intermediate timing between the i-th (i: an integer of 1 or larger) switch timing and the (i+1)th switch timing of the clock signal input to said clock input terminal;

2. (Previously Presented) The semiconductor integrated circuit according to claim 1, wherein said internal clock generating circuit includes:

first means for holding a delay amount corresponding to a time which is equal to half of the difference between the (i-j)th switch timing and the (i+1+j)th (j: an integer of 0 or larger) switch timing of the clock signal (an amount corresponding to switching of (2j+1) times); and

second means for generating said internal clock by delaying said clock signal only by a time equal to said held delay amount.

3. (currently amended) The semiconductor integrated circuit according to claim 1, wherein said internal clock generating circuit is ~~constructed by~~comprised of first and second frequency dividers, a phase comparator, a variable delay circuit, and a delay control circuit and comprises:

said first frequency divider for generating a first frequency divided signal synchronized with the (i-j)th switch timing of said clock signal;

said second frequency divider for generating a second frequency divided signal synchronized with the (i+1+j)th switch timing of said clock signal;

said phase comparator for comparing the phase of said first frequency divided signal and the phase of said second frequency divided signal; and

said delay control circuit for controlling said variable delay circuit so as to have delay time corresponding to time which is equal to half of said phase

difference,

wherein said clock signal is input to the variable delay circuit, and an output signal of the variable delay circuit is used as said internal clock signal.

4. (Previously Presented) The semiconductor integrated circuit according to claim 3, further comprising a clock input buffer for receiving a clock signal which is input to said clock input terminal,

wherein said clock input buffer generates a first clock signal and a second clock signal at a level complementary to the first clock signal,

wherein, when said first clock signal is input to said first frequency divider, said second clock signal is input to said second frequency divider, and

wherein, when said first clock signal is input to said second frequency divider, said second clock signal is input to said first frequency divider.

5. (currently amended) A semiconductor integrated circuit comprising:

a clock input terminal;

a data input terminal;

an internal clock generating circuit for generating an internal clock signal from a clock signal which is input to said clock input terminal; ~~and~~

a latch circuit for latching a data signal input to said data input terminal synchronously with said internal clock signal; and

means for preventing a timing margin, at a time of latching the data signal synchronously with said internal clock signal, from being decreased in a case wherein a duty ratio of the clock signal input to the clock input terminal is different than 50%, said means comprising the internal clock generating circuit including:

~~wherein said internal clock generating circuit includes:~~

a first variable delay circuit for receiving said clock signal and outputting said internal clock signal;

a second variable delay circuit for delaying said clock signal or an inversion signal of said clock signal;

a third variable delay circuit for delaying an output signal of said second variable delay circuit;

a first frequency divider for dividing the frequency of an output signal of said third variable delay circuit;

a second frequency divider for dividing the frequency of said clock signal or the inversion signal of said clock signal;

a phase comparator for comparing the phase of a first frequency divided signal output from the first frequency divider with the phase of a second frequency divided signal output from the second frequency divider; and

a delay control circuit for outputting a delay control signal for controlling said first, second, and third variable delay circuits on the basis of an output signal of said

phase comparator,

wherein said first, second, and third variable delay circuits have the same configuration,

wherein said first frequency divider generates a first frequency divided signal that is synchronized with the (i-j)th switch timing of said clock signal (where i denotes an integer of 1 or larger and j denotes an integer of 0 or larger),

wherein said second frequency divider generates a second frequency divided signal that is synchronized with the (i+1+j)th switch timing of said clock signal,

wherein said phase comparator compares the phase of said first frequency divided signal with the phase of said second frequency divided signal to obtain a phase difference, and

wherein said delay control circuit controls the delay times of said first, second, and third variable delay circuits so that said phase difference becomes zero.

6. (currently amended) The semiconductor integrated circuit according to claim 5,

wherein each of said first and second frequency dividers is ~~constructed by connecting~~ comprised of a plurality of latch circuits connected in series ~~and, by~~ and means for setting initial states of the latch ~~circuits, the~~ circuits so that the value of j is set.

7. (Previously Presented) The semiconductor integrated circuit according to claim 5,

wherein the initial state of said latch circuit can be set by a fuse signal or an external input signal.

8. (Previously Presented) The semiconductor integrated circuit according to claim 5,

wherein a dummy delay circuit, having delay time which is twice as long as a time obtained by subtracting the delay time of a signal transmitted from said data input terminal to said latch circuit from the sum of a delay time of a signal transmitted from said clock input terminal to the first variable delay circuit and a delay time of a signal transmitted from the first variable delay circuit to said latch circuit, is disposed on a signal path extending from said clock input terminal to the first frequency divider.

9. (Currently Amended) A semiconductor integrated circuit comprising:

a clock input terminal;

a data input terminal;

an internal clock generating circuit for generating an internal clock signal from a clock signal which is input to said clock input terminal; and

a latch circuit for latching a data signal input to said data input terminal

synchronously with said internal clock signal,

means for preventing a timing margin, at a time of latching the data signal synchronously with said internal clock signal, from being decreased in a case wherein a duty ratio of the clock signal input to the clock input terminal is different than 50%, said means comprising the internal clock generating circuit including:

~~wherein said internal clock generating circuit includes:~~

a variable delay circuit for receiving said clock signal and outputting said internal clock signal;

a dummy variable delay circuit for delaying an output signal of said variable delay circuit;

a first frequency divider for dividing the frequency of an output signal of said dummy variable delay circuit;

a second frequency divider for dividing the frequency of said clock signal or the inversion signal of said clock signal;

a phase comparator for comparing the phase of a first frequency divided signal output from the first frequency divider with the phase of a second frequency divided signal output from the second frequency divider; and

a delay control circuit for outputting a delay control signal for controlling said variable delay circuit and said dummy variable delay circuit on the basis of an output signal of said phase comparator,

wherein said first frequency divider generates a first frequency divided signal

that is synchronized with the (i-j)th switch timing of said clock signal (where i denotes an integer of 1 or larger and j denotes an integer of 0 or larger),

wherein said second frequency divider generates a second frequency divided signal that is synchronized with the (i+1+j)th switch timing of said clock signal,

wherein said phase comparator compares the phase of said first frequency divided signal with the phase of said second frequency divided signal to obtain a phase difference, and

wherein said delay control circuit controls the delay times of said variable delay circuit and said dummy variable delay circuit so that said phase difference becomes zero.

10. (original) The semiconductor integrated circuit according to claim 9, further comprising a memory cell array in which a plurality of memory cells are arranged in an array,

wherein write data to any of said memory cells can be transmitted as said data signal to said latch circuit.